REMARKS

The Office Action dated November 2, 2005 has been received and carefully noted. No claims have been amended, cancelled, or added, and Applicants submit that no new matter has been introduced. As such, claims 9-28 are pending in the application and are submitted for consideration.

Claims 9-16, 19-23, 25, and 27 stand rejected in the Office Action under 35 U.S.C. §102(e) as being anticipated by *Golikeri* (US Publication No. 2003/0067926). The Office Action took the position that *Golikeri* taught each and every element recited in claims 9-16, 19-23, 25, and 27. Applicants traverse the rejection and respectfully submit that each of claims 9-16, 19-23, 25, and 27 recites subject matter that is not taught or disclosed by *Golikeri*.

Independent claim 9 recites a method for improving the reliability of a computer system including a bus and plug-in units coupled thereto. The method includes providing to each of a plurality of plug-in units a separate interface circuit such that each of the plug-in units is connected to the bus via the interface circuit corresponding thereto. The method further includes addressing a respective plug-in unit, via the bus, by addressing operations directed at that respective plug-in unit and which are monitored by the interface circuit corresponding thereto. Further still, the method includes performing a time duration operation of addressing of said plug-in unit, and checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before

expiration of a predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing, and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to that plug-in unit is terminated by the interface circuit corresponding thereto by sending into the bus a signal indicating termination of addressing.

Independent claim 13 recites an interface circuit for providing local monitoring capability to a plug-in unit of a computer system including a bus and plug-in units coupled to the bus, wherein a separate interface circuit is provided to connect each of the plug-in units to the bus. The interface circuit includes a watchdog timer, first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of the addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

Independent claim 21 recites a computer system including a bus and plug-in units coupled thereto. The computer system includes a plurality of interface circuits and a plurality of plug-in units, each of which is connected to the bus via a separate one of the interface circuits corresponding thereto. Each of the interface circuits includes a watchdog timer, first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for

sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of the addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer.

Golikeri teaches a system for address management in a distributed communication environment, wherein the system is configured to purge obsolete addresses from an address table for modules in the system. The system of *Golikeri* generally includes a number of address databases distributed across one or more communication devices. Each address database is maintained independently by a module, and the various modules are interconnected by a bus or backplane so that the modules can coordinate address management across the distributed address databases. In *Golikeri*, each module monitors the status of its locally owned address entries in order to identify any locally owned address entries that become obsolete. A locally owned address entry may be considered obsolete if no protocol messages are sent to or from the corresponding directly connected communication device within a predetermined period of time. When a module determines that a locally owned address entry is obsolete, the module purges the locally owned address entry from its address database, and then sends a purge message to the other modules including the obsolete address from the purged address entry. Upon receiving the purge message, the other modules purge the corresponding remotely owned address entry from their respective address databases, thereby synchronizing their respective address databases. Each module may also periodically send a keep-alive message to the other modules identifying each locally owned address that the module

considers to be active. Each module also maintains a timer for each remotely owned address entry. A module resets the timer for a particular remotely owned address entry each time the module receives a keep-alive message indicating that the corresponding address is active. The module purges a particular remotely owned address entry if the corresponding timer expires by reaching a predetermined timeout value. Thus, each module eventually purges an obsolete address entry, even if the purge message was not received by all modules.

Upon careful review of *Golikeri*, Applicants submit that each and every limitation recited in claims 9-16, 19-23, 25, and 27 is not taught or disclosed by *Golikeri*.

With regard to independent claim 9, Applicants submit that this claim recites elements that are not taught or disclosed by *Golikeri*. More particularly, claim 9 recites an interface circuit positioned between the bus and each of the plug-in units, which is not disclosed or taught by *Golikeri*. Further, claim 9 recites that the interface circuit monitors the addressing of the plug-in unit, which is not disclosed or taught by *Golikeri*. The Office Action cites to paragraph 36 of *Golikeri* as teaching the interface circuit limitation, however, Applicants submit that careful review of paragraph 36 does not support this conclusion. Applicants submit that paragraph 36 teaches that "various modules are interconnected, for example, via a bus, backplane, or other signaling medium, so that the modules can coordinate address management across the distributed address database." Paragraph 36 makes no mention of an interface circuit or an interface circuit monitoring addressing of plug-in units. Further still, claim 9 recites a time duration operation of

addressing the plug-in units, whereby, the state of addressing of the plug-in units is checked by timing, and when a time duration of addressing is exceeded, the addressing to the specific plug-in unit is terminated. This feature is also not taught or disclosed by *Golikeri*, as *Golikeri* teaches timing the duration an address resides in an address table to determine when an address is no longer used, while the claimed invention is directed to monitoring the duration that a particular device is being addressed by another device through the bus. When a device is being addressed or called for more than a predetermined duration, the invention recognizes this event and terminates the addressing function, which prevents the system from becoming paralyzed in a continual addressing state. This feature is distinct from the address table synchronization of *Golikeri*. As such, Applicants submit that *Golikeri* fails to teach or disclose each and every element recited in independent claim 9. Reconsideration of the rejection of claim 9, along with dependent claims 10-12, and 20 is respectfully requested. In the event that the Office Action maintains the rejection over Applicants traversal, Applicants respectfully request that the Office Action point out the specific sections of *Golikeri* that teach the features discussed above.

With regard to the rejection of independent claim 13, Applicants submit that claim 13 recites subject matter that is not disclosed or taught by *Golikeri*. More particularly, *Golikeri* fails to teach means for activating a watchdog timer upon startup of an addressing operation directed to a plug-in unit (as discussed above with respect to claim 9). Further, *Golikeri* fails to teach a second means for sending into the bus a signal

indicating termination of the addressing process when the duration of the addressing exceeds a predetermined time duration as measured by the watchdog timer. As noted above, *Golikeri* is directed to synchronizing address tables based upon the age of an address in the table, while the claimed invention is directed to timing an addressing process to determine when the addressing process has gotten stuck in an indefinite loop, and the invention stops the indefinite loop after a watchdog timer times out. Thus, Applicants submit that independent claim 13 recites subject matter that is not taught or disclosed by *Golikeri*. Reconsideration of the rejection of claim 13, along with dependent claims 14-19, is respectfully requested.

With regard to the rejection of independent claim 21, Applicants submit that claim 21 recites limitations that are not taught or disclosed by *Golikeri*. More particularly, claim 21 recites providing a plurality of interface circuits connected between the plug-in units and the bus. The interface circuits include a watchdog timer, means for activating the timer when an addressing operation starts, and means for sending an addressing termination signal to the bus when the timer determines that the addressing operation has reached a predetermined duration. These features are not disclosed in *Golikeri*, and as such, reconsideration of the rejection of claim 21, along with dependent claims 22-28 is respectfully requested.

In sum, Applicants submit that *Golikeri* fails to teach the hardware or methodology of terminating an addressing process, as recited in the present claims. Rather, *Golikeri* is directed to outside monitoring and synchronizing addressing tables,

which is distinct from the internal self monitoring addressing process of the present invention where each peer is locally monitored by themselves. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 17-18, 24, 26, and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Golikeri* in view of *Microsoft Computer Dictionary*. The Office Action took the position that *Golikeri* teaches each and every limitation recited in claims 17-18, 24, 26, and 28, with the exception of the Compact PCI bus. However, the Office Action cited to the definition of a Compact PCI bus from the *Microsoft Computer Dictionary* and took the position that it would have been obvious for one of ordinary skill in the art to combine the teaching of the references to render the rejected claims obvious. Applicants traverse the rejection and respectfully submit that the cited combination of references fails to teach, show, or suggest each and every limitation recited in claims 17-18, 24, 26, and 28.

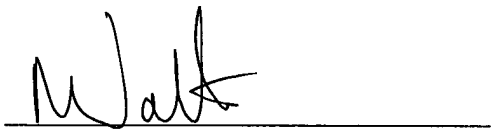
More particularly, each of claims 17-18, 24, 26, and 28 recite an interface circuit, which, as discussed above, is not taught, shown, or suggested by the *Microsoft Computer Dictionary*. Further, each of the rejected claims recite timing the duration of an addressing process with a watchdog timer, as discussed above, which is also not taught by *Microsoft Computer Dictionary*. Therefore, Applicants submit that the *Microsoft Computer Dictionary* fails to further the teaching of *Golikeri* to the level necessary to properly support an obviousness rejection. Reconsideration and withdrawal of the rejection is respectfully requested.

In conclusion, Applicants submit that the cited references, taken alone or in combination, fail to teach, show, or suggest each and every limitation recited in claims 9-28. These claims are directed to monitoring an addressing process to make sure the process does not get stuck in a continuous loop trying to address a unit, where the cited references are directed to synchronizing an address table. Applicants submit that these processes are separate and distinct from each other. Reconsideration and withdrawal of the rejection of pending claims 9-28 is therefore respectfully requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



N. Alexander Nolte
Registration No. 45,689

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

NAN:kzw